

REMARKS

The present application relates to a semiconductor device that includes a capacitor provided on a supporting substrate including an integrated circuit. The capacitor includes a lower electrode, a dielectric film, and an upper electrode. A first interlayer film is provided to cover the capacitor, and a first interconnect is provided on the first interlayer film connecting the integrated circuit and the capacitor through a hole formed in the first interlayer insulating film. A second interlayer, having a tensile stress, is provided to cover the first interconnect and the first interlayer insulating film. A second interconnect is provided on the second interlayer insulating film, and is electrically connected to the first interconnect through a hole formed in the second interlayer insulating film. A passivation layer is also provided to cover the second interconnect.

Reconsideration and allowance of claims 1-2, "rejected under 35 U.S.C. § 102(b) as being clearly anticipated by Applicant's Specification", are respectfully requested..

Claim 1 has been amended to specify that a first interlayer insulating film is provided "so as to directly cover the capacitor." This feature is found in the originally filed application at Figure 1B, and at page 17, lines 21-23. Claim 1 has also been amended to specify that a second interlayer insulating film "having a tensile stress" is "provided so as to directly cover the first interconnect and the first interlayer insulating film." This feature is found in the originally filed application at Figure 1C, page 19, lines 3-5, and at page 32, lines 9-21. No new matter has been added by the amendments to claim 1.

The semiconductor device described in Applicants' specification, through Figures 10A-10E, is very different from the semiconductor device recited in claim 1. The semiconductor device described with reference to Figures 10A-10E includes a second interlayer insulating film that is formed of a plasma TEOS film, and therefore has a compressive stress (See specification, page 4, line 19 through page 5, line 8). In contrast, the second interlayer insulating film recited in claim 1 is formed of an ozone TEOS film, and, therefore, has a tensile stress (See specification, page 12, lines 5-17). As defined in the specification, an insulating film having a compressive stress

includes "a force for expanding the layer," while an insulating film having a tensile stress includes "a force for contracting the layer" (See specification, page 5, lines 11-16).

It is important that the second interlayer insulating film recited in claim 1 has a tensile stress, and not a compressive stress. The compressive stress of a film prevents the polarization of the dielectric material forming the dielectric film 8 in the capacitor 10. Accordingly, the characteristics of the capacitor 10 are improved when the second interlayer insulating film has a tensile stress, as opposed to a compressive stress (See specification, page 6, lines 4-16, and page 12, lines 10-17). Therefore, claim 1, as amended, is patentable over the semiconductor device illustrated by Applicants' Figures 10A-10E because claim 1 defines a semiconductor device that is different from the semiconductor device illustrated by Applicants' Figures 10A-10E and the differences provide meaningful benefits and advantages.

Claims 3-4, 6 and 10 stand "rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Specification in view of Yoshizumi et al. (US Patent No. 5,444,012)." Further, claims 5 and 7-9 stand "rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Specification in view of Matsuura et al. (US Patent No. 5,132,774)." As discussed below, neither Yoshizumi et al., nor Matsuura et al., include the above-recited features of claim 1 that distinguish claim 1 from Applicants' specification.

Yoshizumi et al. teaches a method of depositing a silicon oxide film that includes a first silicon depositing step on a bonding pad, a step of exposing the bonding pad by etching, and a second silicon depositing step (See Yoshizumi et al., Abstract). Therefore, a fuse element is covered by both the first and the second depositing steps, and the bonding pad is only covered by the second depositing step (Abstract). Yoshizumi et al. does not teach an insulating film having a tensile stress, and is, therefore, very different from Applicants' semiconductor device as recited by claim 1.

Matsuura et al. teaches a method of forming an interlayer insulating film that insulates first and second layers of conductor patterns in a semiconductor device (See Matsuura et al., Abstract). Matsuura et al. does

teach a TEOS APCVD film 14 that has tension stress; however, Matsuura et al. teaches to relax the stress in metal conductor 12 by sandwiching film 14 between an upper and a lower insulating film 13 and 16 (See Matsuura et al., Column 6 line 64 through Column 7, line 6 and illustrated in Figure 5B). Therefore, the film 14 is not provided directly on the conductor 12, as the insulating film 13 is provided between them (Figure 5B). Because the films 13 and 16 are formed using silane gas and nitrous oxide, TEOS and O<sub>2</sub>, or as a PSG film using gas that has phosphine added to silane gas and O<sub>2</sub>, the films 13 and 16 have compressive stress (See Matsuura et al., Column 7, lines 3-15). As such, the Matsuura et al. reference suffers from the same compressive stress problems previously described by reference to Figures 10A-10E of the present application.

In contrast, amended claim 1 includes the feature of the first interlayer insulation film being “provided so as to directly cover the capacitor”. Therefore, in claim 1, there is no insulating film that has a compressive stress between the conductor (capacitor 10, with electrode 9) and the interlayer insulating film that has tensile stress. As such, claim 1 does not suffer from the deteriorated capacitor characteristics included in Matsuura et al. and the prior art illustrated by Figures 10A-10E of the present application. Consequently, even by combining Matsuura et al. and the semiconductor device described in Applicants’ specification (and illustrated by Figures 10A-10E), Applicants’ claimed device is not achieved.

Therefore, Applicants’ invention, as defined by claim 1, is patentable over any combination of Applicants’ specification, Yoshizumi et al. and Matsuura et al. Claims 2-10 include all of the features of independent claim 1 from which they depend. Therefore, claims 2-10 are also patentable over any combination of Applicants’ specification, Yoshizumi et al. and Matsuura et al.

Consideration and allowance of newly added claim 28 is respectfully requested. Claim 28 includes the feature of a “...hydrogen supplying layer provided between the first interconnect and the second interlayer insulating film...”. As recited by claim 1, the hydrogen supplying layer has a sufficient amount of hydrogen “for repairing damage done to the integrated circuit caused in forming the first contact hole...” This means that damage done to the integrated circuit during the process of dry etching the first contact hole is repaired by the inclusion of the hydrogen supplying layer, since the hydrogen

supplying layer includes a sufficient amount of hydrogen to repair the damage. This feature is found in the originally filed application at page 18, lines 10-30. No new matter has been added.

The Office Action provides that Matsuura et al. includes a hydrogen supplying layer (insulating layer 13 in Figure 5B). However, Matsuura et al. does not indicate that the insulating layer 13 includes sufficient hydrogen to repair damage done to the integrated circuit during the formation of the first contact hole. Matsuura et al. only discloses that the insulating layer 13 is formed by using silane gas and nitrous oxide, by using TEOS and O<sub>2</sub>, or by using gas that has phosphine added to silane gas and O<sub>2</sub> (See Matsuura et al., Column 7, lines 7-15).

It is because Applicants include the recited hydrogen supplying layer that the following advantages are achieved. The integrated circuit 4 is able to recover from damage caused during the dry etching performed to form the first contact hole (See specification, page 18, lines 17-30).

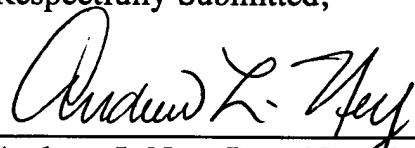
Accordingly, for the reasons set forth above, claim 28 is patentable over Applicants' specification in view of Matsuura et al.

In view of the amendments and arguments set forth above, the above-identified application is in condition for allowance which action is respectfully requested.

Request for Extension of Time:

In the subject application, it is requested that the shortened period for responding to the Official Action dated January 30, 2001 be extended one month until May 30, 2001. Enclosed is the Patent Application processing fee under 37 C.F.R. § 1.17.

Respectfully Submitted,



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CS:aw

Enclosures:

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Dated: May 30, 2001

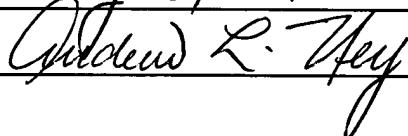
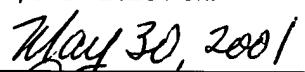
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VERSION WITH MARKINGS TO SHOW CHANGES MADECLAIMS:

1. (Once Amended) A semiconductor device, comprising:
  2. a capacitor provided on a supporting substrate having an integrated circuit thereon and including a lower electrode, a dielectric film, and an upper electrode;
  5. a first interlayer insulating film provided so as to directly cover the capacitor;
  7. a first interconnect selectively provided on the first interlayer insulating film and electrically connected to the integrated circuit and the capacitor through a first contact hole formed in the first interlayer insulating film;
  11. a second interlayer insulating film having a tensile stress [formed of ozone TEOS and] provided so as to directly cover the first interconnect and the first interlayer insulating film;
  14. a second interconnect selectively provided on the second interlayer insulating film and electrically connected to the first interconnect through a second contact hole formed in the second interlayer insulating film; and
  17. a passivation layer provided so as to cover the second interconnect.

Claim 28 has been added.